Methods of Programmable Amplitude of Portable Electrical Stimulator for Multi-channel FES

Rachmad Setiawan
Jurusan Teknik Elektro
Fakultas Teknologi Industri, Institut Teknologi Sepuluh Nopember (ITS), Surabaya, Indonesia
e-mail: rachmad@ee.its.ac.id

Achmad Arifin
Jurusan Teknik Elektro
Fakultas Teknologi Industri, Institut Teknologi Sepuluh Nopember (ITS), Surabaya, Indonesia
e-mail : arifin@ee.its.ac.id

***Abstract*— Fundamental research about Functional Electrical Stimulation (FES) indicates that FES can be used to rehabilitate motoric system of patient experiencing damage at arrangement of central nerve resulted from cerebrospinal of cord injury (SCI) and also stroke. To generate impulse to human body organ activated by FES is difficult and very complex because of nonlinearity response from neuromuscular system, various response of musculoskeletal system such as having long time delay and fatigue phenomenon (muscle fatigue). Therefore, an open-looped control system is inappropriate to employ. Close-looped control is feasibly appropriate to overcome this constraint in FES appliance to yield accurate impulse generator. For the application of closed-loop control at clinical level, FES system must be designed using portable multi-channel device to pleasant the patient. In this research, the realized FES stimulator is designed by employing a highly linear boost converter circuit using fixed frequency and duty cycle ranging from 0% to 25%, because it yields relatively linear and higher output voltage swing than FES controlled by frequency.**

Keywords— Functional Electrical Stimulation (FES), closed-loop control, boost converter, duty cycle.

I. Introduction

Functional electrical stimulator (FES) has been widely used in rehabilitation of ability of motoric system of patient experiencing damage at arrangement of central nerve resulted from cerebrospinal of cord injury (SCI) and also stroke. Researches about FES at clinical level include covers rehabilitation of kinetic performance on upper side of man kinetic organs (upper limb) and also under (lower limb) in everyday life, like grasping [1][2], standing up and walking / running (gait) [2][3]. In Indonesia, many paralysis patients experiencing losing of performance to run resulted by trouble in motoric nervous system as result of cerebrospinal of cord injury or damage at brain (brain damage). Therefore, FES is very potentially important to be developed as one of rehabilitation methods in motoric system. The application of FES for rehabilitation of running performance at clinical level in general applies system triggered manually by applying an open-looped control. This system is commonly used regarding to its simple and easy to develop.

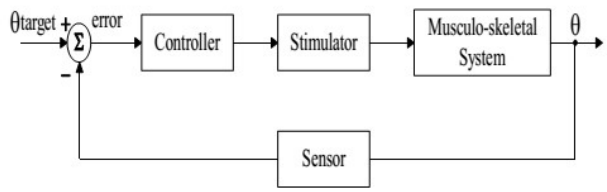

Figure 1. A closed-loop FES system diagram

Basically, an open-looped FES does not exploit muscle model to predict cupola from electrical stimulation intensity. FES system with control open-loop can yield good impulse only in condition of the controlled musculoskeletal system is unchanged. Human body organs activated by FES require a reliable operation method so it can yield desired impulse response. However, controlling human body organ activated by FES is difficult and very complex because of the nonlinearity response from neuro-muscular system, various from response musculoskeletal system to electrical stimulation, long time delay, and fatigue phenomenon (muscle fatigue). Therefore, to overcome constraints in FES controller, an application of closed-loop control system to yield accurate impulse is required.

In this research, development of portable multi-channel FES system to counterpart problems in the lack of supporting facilities for rehabilitation motoric system at clinical level by using closed-loop control. Typical closed-loop FES system consists of a controller, a stimulator and a sensor system, like depicted at Figure 1.

II. Theoritical Background

Some methods to change DC voltage level to become DC voltage in which its amplitude differs among others are buck converter, boost/burst converter, buck-boost converter, and cuk converter. Many former papers have discussed different methods of dc-to-dc conversion.

From the earlier paper in [4], dc-to-dc conversion method in accordance with the desired design is a boost conversion method. In this research, we have designed a boost converter circuit. The boost converter or step -up converter is a dc-to-dc converter functioned to boost-up a dc voltage level to higher level. Ideal boost converter circuit consists of principal

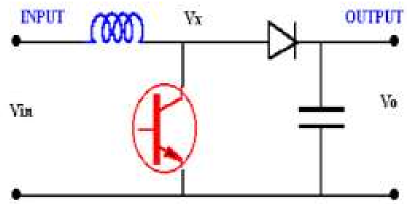

Figure 2. Basic Scheme of Boost Converter

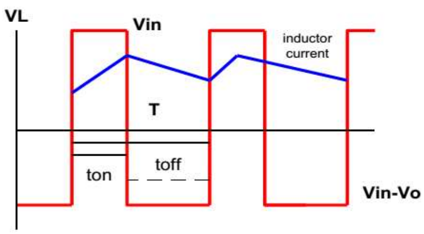

Figure 3. Voltage and current waveform

components that is intrinsic semiconductor switches, diode, inductor and capacitor.

Figure 2 shows a boost fundamental converter circuit using a transistor as a switch. This circuit is applied when a higher level output voltage than input is required. Analytically, when transistor is in ON state, the voltage in node Vx is equal to Vin and the system state is in OFF condition, the inductor current flows towards to diode and gives Vx = Vo. To analyze this scheme, the inductor current is assumed to be flowing. Thus, the voltage passing through the inductor shown in Figure 2 and its average current must be zero, so that it will be remaining at condition of steady state. It can be formulated as in equation (1).

$$V_{in}t_{on} + (V_{in} - V_o)t_{off} = 0 \quad (1)$$

Equation (1) can be rearranged become,

$$\frac{V_O}{V_{in}} = \frac{T}{t_{off}} = \frac{1}{(1-D)} \quad (2)$$

And for lossless circuit regarding to conservation of energy, Equation (2) can be expressed as

$$\frac{I_O}{I_{in}} = (1 - D) \quad (3)$$

Since the value of duty ratio "D" is between 0 and 1, the output voltage magnitudes must be always higher than its input voltage. The negative sign shows the inversed output voltage.

The FES which will be proposed uses a method of boost/burst converter since:

- The wanted output voltage starts out of 50 Vdc up to 120 Vdc; this is a type of step-up converter.
- Ground applied by 1 so that output voltage applied must as of phase.
- The wanted designs can be as small as possible. Thus, the capacitor value for boost/burst converter circuit must be small in value.

In scheme of circuit boost converter with above constraints of input voltage, output voltage and load current, the value of L is the first parameter which is determined using formula in equation (4).

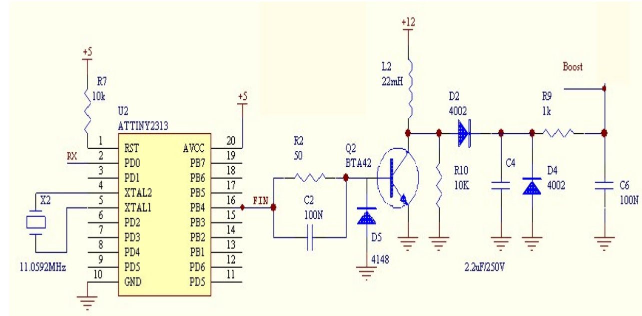

Figure 4. Amplitude generator circuit of FES

$$L = \frac{(V_{out} - V_{in} + V_D)(1-D)}{i_{load} \cdot f} \quad (4)$$

where V_D is diode voltage, D is duty cycle and f is frequency. In this paper, the boost converter designed is equipped with desired parameters:

1. Input voltage of 5 V
2. Output voltage of 100 V
3. Frequency between 0 - 500 Hertz
4. Duty cycle = 50 %
5. Load current 5 mA (Maximum current 60 mA)

From above parameters, the inductor value can be calculated by using the formula in equation (4). As a result, the inductor value is 19.14 mH. Inductor of 22 mH is then used which is easily available in the market.

Furthermore, to find the capacitor value that is used for speeding up the circuit response, equation (5) is used. The calculation of the capacitor Cs is done in (6). To fulfill the required parameter, the value of Cs must be less than 2 µF. Here, 100 nF capacitor is chosen to be applied regarding to its small size.

$$C_s < \frac{1}{20.R_B.f_{max}} \quad (5)$$

$$C_s < \frac{1}{20.50.500}, C_s < 2\mu F \quad (6)$$

To determine transistor type which will be applied to the circuit, a calculation using equation (7) is used.

$$f_{max} = \frac{0.35}{100.t_r} \quad (7)$$

where t_r (recovery time) is time required by transistor for transition condition from cut off becomes saturation. If we set the f_{max} to be 500 Hz, we will obtain t_r = 7µs. From this calculation of t_r, a MMBTA42 transistor is chosen and applied to the circuit, since the rise time (t_r) from MMBTA42 datasheet is 15 ns.

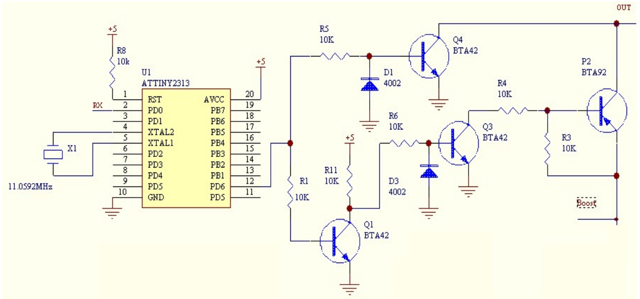

Figure 5. Pulse generator circuit of FES

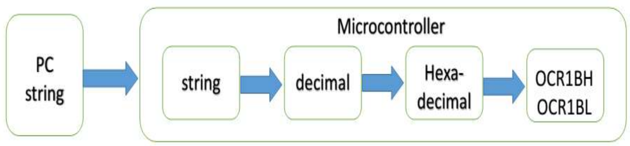

Figure 6. Data conversion flow of software design

III. Design Implementation

The FES system design consists of hardware and software designs.

A. Hardware design

Multi-channel FES, each channel consists of two main parts: an amplitude generator as depicted in Figure 4 and a pulse generator as depicted in Figure 5. The core circuit of the proposed FES is capable to yield output signal in the form of modulation. An ATTiny2313 microcontroller is employed to the pulse generator and amplitude generator. Output of pin 12 (PD6) directly is disjointed to become 2 line, one of them is channeled through a transistor MMBTA42 (Q4), while the other in advance is channeled to a transistor MMBTA42 (Q1) as an inverter before it is finally connected to MMBTA42 (Q3). In the second part (the lower part of the circuit), collector output of Q3 is connected to the base of MMBTA92 (P2). As a result, this combination with Q4 and P2 yields larger modulation of voltage output.

The modulation duration can be easily controlled by software programming at microcontroller. Meaning, the on time t_{ON} modulation is in rising edge and the off time t_{OFF} modulation is in falling edge, it is fully done by microcontroller commanded by user through a personal computer/laptop. A Bluetooth tool is used to transmit and receive data to and from the FES module with baudrate setting of 115200 bps. Since the Bluetooth has a data input type of TTL level, it is required a USB to TTL converter.

B. Software design

The duty cycle data transmitted from computer must be converted into a string of data for following serial communication data format, while the duty cycle data of the microcontroller must be in hexadecimal data high and hexadecimal data low. To convert the data into a hexadecimal string can be obtained by receiving a string of data first, and then used as a decimal, afterward it is converted into hexadecimal data high and hexadecimal data low. Figure 6 shows the sequence of data conversion in string format to be hexadecimal.

Figure 7. The proposed pulse generator circuit of FES

First procedure, the microcontroller of ATTiny2313 has to be initialized to activate its serial data communication with 115200 bps, with parameter of 8 data, 2 stops and no parity. Since we have 2 duty cycle data, then any data must be sent in the form of characters of different protocols e.g. 'a' and 'c'. For ATTiny 2313, timer 1 is used with fast Pulse Width Modulation (PWM) coded as follows,

$$Foc1a = Fosc/(N*(1+TOP))$$
$$Foc1b = Fosc/(N*(1+TOP))$$
$$D = (OCR1X/TOP)*100\%$$

where:

Foc1a = Frequency output OC1A
Foc1b = Frequency output OC1B
N = Clock Scale (1, 8, 64, 256 and 1024)
D = Duty cycle
Fosc = Crystal Frequency
TOP = maximum counter (TCNT1), TOP0 has 3 values that is 8 bits (FF), 9 bits (1FF) and 10 bits (3FF)

To determine the duty cycle, we use the following calculation in software:

$$D = (OCR1X/TOP)*100\%$$
$$75\% = (OCR1X/1023)*100\%$$
$$OCR1X = 767 = 2FF \text{ (in hexadecimal)}$$

Second procedure, the microcontroller of ATTiny2313 has to be initialized to yield frequency output and duty cycle = 0%. Third procedure, we create a software program to receive serial data in string and then convert the data string to decimal. In order to yield duty cycle, decimal data converted into hexadecimal. Finally, the hexadecimal data is divided into 2 groups, high hexadecimal and low hexadecimal.

IV. Experimental Results

Figure 7 shows the photograph of the proposed multichannel FES stimulator. To show the performance of the proposed FES, experimental tests by giving frequency inputs of 84 Hz, 168 Hz, and 337 Hz with duty cycle 0% to 25%. Table 1 summarizes the measurement results. For input frequency of 84 Hz, the output voltage changes transiently from 0% until 12% duty

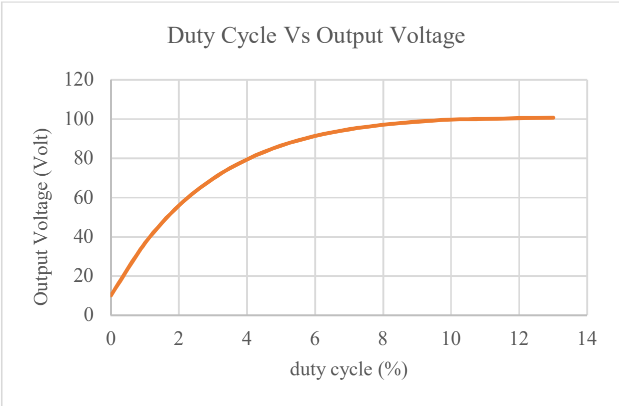

Figure 8 FES output for frequency input of 84 Hz with duty cycle 0% to 13%

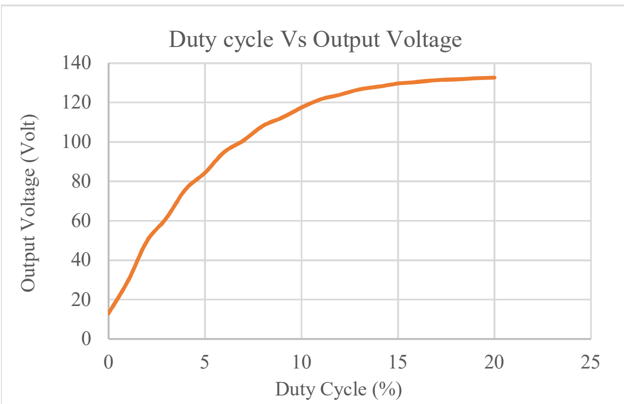

Figure 9 FES output for frequency input of 168 Hz with duty cycle 0% to 20%

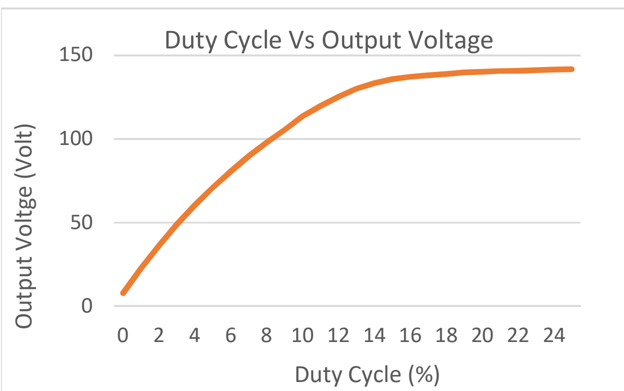

Figure 10 FES output for frequency input of 337 Hz with duty cycle 0% to 25%

cycle, while in duty cycle of 13% and above, the output voltage become constant as depicted in Figure 8. Linear output voltage is generated if the duty cycle input of 1% to 4%.

For input frequency of 168 Hz, the output voltage changes transiently from 0% until 19%, while in duty cycle of 20% and above, the FES generates constant output voltages as depicted in Figure 9. Linear output voltage is generated if the duty cycle input of 1% to 10%. For input frequency of 337 Hz, the output voltage changes transiently from 0% until 24%, while in duty cycle of 25% and above, the FES generates constant output

TABLE 1 Measurements of FES for three frequency inputs

Frequency = 84 Hz		*Frequency = 168 Hz*		*Frequency = 337 Hz*	
Duty Cycle (%)	**Output Voltage (volt)**	**Duty Cycle (%)**	**Output Voltage (volt)**	**Duty Cycle (%)**	**Output Voltage (volt)**
0	10.15	0	13.01	0	7.87
1	36.81	1	29.23	1	22.66
2	56.02	2	49.75	2	36.39
3	69.70	3	61.31	3	48.95
4	79.50	4	76.00	4	60.46
5	86.50	5	84.30	5	71.00
6	91.40	6	94.80	6	80.70
7	94.80	7	100.70	7	89.70
8	97.10	8	108.10	8	97.90
9	98.70	9	112.30	9	105.40
10	99.80	10	117.40	10	113.60
11	100.10	11	121.60	11	119.80
12	100.50	12	123.90	12	125.40
13	*100.70*	13	126.60	13	130.00
14	*100.70*	14	128.00	14	133.40
15	*100.70*	15	129.60	15	135.80
16	*100.70*	16	130.40	16	137.20
17	*100.70*	17	131.30	17	138.10
18	*100.70*	18	131.70	18	138.90
19	*100.70*	19	132.20	19	139.70
20	*100.70*	*20*	*132.60*	20	140.1
21	*100.70*	*21*	*132.60*	21	140.6
22	*100.70*	*22*	*132.60*	22	140.9
23	*100.70*	*23*	*132.60*	23	141.2
24	*100.70*	*24*	*132.60*	24	141.5
25	*100.70*	*25*	*132.60*	25	141.7

voltages as depicted in Figure 10. Linear output voltage is generated if the input duty cycle of 1% to 15%. From this experitments, the prosposed stimulator is reliable for multichannel FES with fixed frequency and duty cycle tuning.

V. CONCLUSION

The proposed multichannel FES stimulator has a boost converter as a primary circuit. The output voltage can be adjusted with the boost converter input frequency and duty cycle. If the input frequency is used, the output voltage generated is not linear, whereas if the input is used duty cycle with a frequency fixed, the output voltage produced linear scale from 0% to a certain scale depending on frequency used. The linearity of the output voltage of the FES will be even wider, if the input frequency used is increasingly higher. However, a constraint encountered when raising the input frequency, the inductor will become hot that lead to inefficient loss in power dissipation. Besides his frequency generator is generated by the microcontroller which is limited by a timer function. So, the realized FES stimulator was a boost converter with fixed frequency and duty cycle from 0 % to 25%, because it yielded relatively linear and higher output voltage than FES controlled by frequency. Therefore, FES will be used for the provision of the stimulus waveform using FES with input duty cycle.

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